Wissenschaftliche Arbeiten und Patente

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P. Klein, K. Hoffmann, B. Lemaitre
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"A Non-Linear Description of the Bias Dependent Parasitic Resistances of Quarter Micron MOSFETs"
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E. Gondro, P. Klein, F. Schuler
"An Analytical Source-and-Drain Series Resistance Model of Quarter Micron MOSFETs and its Influence on Circuit Simulation"
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R. Thewes, R. Brederlow, C. Schlünder, P. Wieczorek, A. Hesener, B. Ankele, P. Klein, S. Kessel, W. Weber
"Device Reliability in Analog CMOS Applications"
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F. Schuler, M. Kerber, P. Klein, W. Molzer, A. v. Schwerin, and G. Tempel
" Long Time Estimation of Failure Rates due to low Temperature Charge Loss"
2000 Non-Volatile Semiconductor Memory Workshop, IEEE 2000 NVSMW.

P. Klein, F. Schuler
"A New Mobility Model for Circuit Simulation in Pocket Implanted MOSFET's"
ICMTS 2000.

G. Knoblinger, P. Klein, U. Baumann
"Thermal Channel Noise of Quarter and Sub-Quarter Micron NMOS FET's"
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G. Knoblinger, P. Klein, M. Tiebout
"A New Model for Thermal Channel Noise of Deep Submicron MOSFET's and its Application in RF-CMOS Design"
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E. Gondro, O. Kowarik and P. Klein
"When do we need Non-Quasistatic CMOS RF-Models?"
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G. Knoblinger, P. Klein, M. Tiebout
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IEEE Transactions on Solid State Circuits, Vol. 36, No. 5, May. 2001, pp. 831 - 837.

P. Klein and S. Chladek
"A New Surface Mobility Model for Pocket Implanted Quarter Micron n-MOSFET's and Below"
8th IEEE International Conference on Electronics Circuits and Systems, ICECS 2001

Dissertation:

Peter Klein
"Analytisches LDDMOS-Transistor Ladungsmodell für CAD-Anwendungen"
Dissertation, Februar 1996.

Patente/Patentanmeldungen:

Mehrere Patente / Patentanmeldungen auf den Gebieten der Halbleitertechnologie und der analogen / HF-analogen Schaltungstechnik

- *"Realisierung integrierter Kapazitäten hoher Güte mittels schmaler, dicht gepackter Verdrahtungsleitungen auf einer oder mehreren Metallisierungsebene(n)"*
- *"Strom-Interface nach CMOS - Mischern"*
- *"An active, linear, low-noise zero- or low-intermediate frequency (IF) mixer"*
- *"A high dynamic, low noise CMOS transconductance mixer using low voltage MOS transistors"*
- *"A low power, low noise CMOS direct down conversion demodulator for mobile communications"*

Veröffentlichungen/Beiträge zu Europäischen Förderprojekten:

P. Klein, K. Hoffmann, B. Lemaitre
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Jessi AC 41 Verbundprojekt, Technology Assessment, Final Report, Phase 2, 1992-1994, Förderkennzeichen 01 M 2871 G.

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Mehrere Vorträge/Beiträge in internationalen Kreisen/Gremien:

Diverse Vorträge auf den Meetings des Compact Model Councils (CMC), Homepage: http://www.eigroup.org/cmc/

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